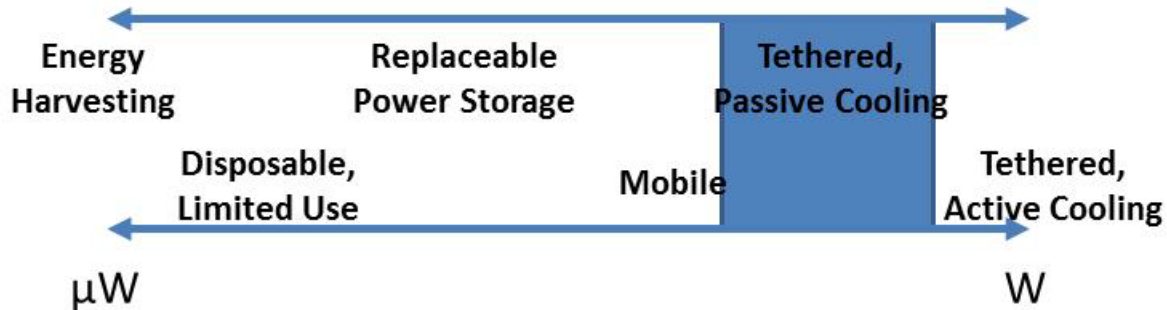


Low Power Optimization Datasheet for Freescale P1022 / QorIQ processor

1. These processors target the shaded portion of the low power spectrum.



2. Operating voltages:

Core: 1 V

I/O: 1.5 V to 3.3 V

3. Typical power at maximum operating frequency

6W at 1.2 GHz (dual-core)

4. These processors include support multiple domains for clock gating. No additional granularity information is available.

5. The P1022 supports Deep Sleep, Jog, and Full Power operating modes.

6. The P1022 supports multiple supply voltages for the core, DDR, PLL, I/O's, and Deep Sleep Power operation.

7. The P1022 supports programmable clock multipliers for frequency scaling. The processor also supports voltage scaling.

Low Power Optimization Datasheet for

Freescle

P1022 / QorIQ processor

8. The included hardware accelerators include functions for encryption, Data Path, and networking header cache stashing.
9. The P1022 does not support multithreading or hardware context switching.
10. The P1022 includes dual e500 Power Architecture cores with an optimized platform interconnect, a hardware cache coherency module, and unified L2 memory.
11. More information for low power software techniques on the P1022 is available to developers from Freescle under NDA.
12. The P1022 includes these additional features to support low power designs:
 - A. The P1022 has the networking and platform logic powered in deep sleep mode to allow it to appear to be active on the network. P1022 based systems are fully network discoverable in the deep sleep mode and it processes incoming messages with similar behavior compared to a fully powered system.
 - B. The P1022 has low deep sleep power that enables a system solution that consumes less than 1W as measured at the AC wall plug as required by upcoming EnergyStar and EuP mandates. While in the deep sleep power state, incoming messages are received and put thru hardware filters and then as appropriate put into DRAM without any packet loss. The P1022 transitions to a full power state when the filter logic passes messages into DRAM. All of this occurs while maintaining the network behavior of a fully powered system to outside devices.