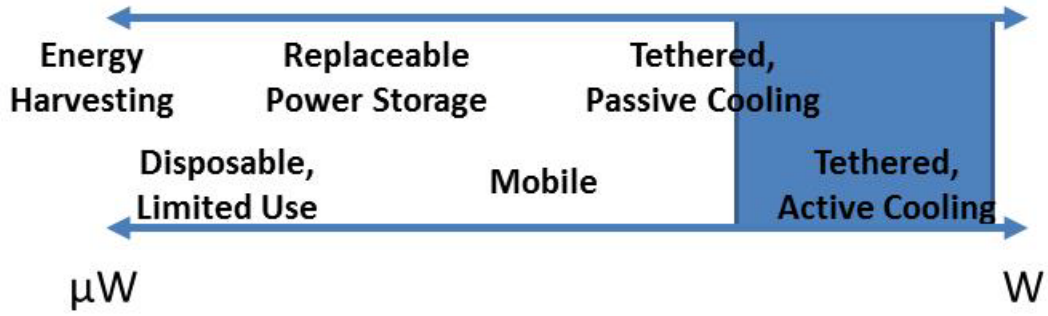
Low Power Optimization Datasheet for

Texas Instruments C6-Integra DSP + ARM processors

1. The C6-Integraprocessors target the shaded portion of the low power spectrum.



2. Operating voltages:

0.9V, 1V AVS (SmartReflex Technology), 1V constant,

1.5V, 1.8V, 3.3V

3. Typical power at maximum operating frequency

1.2GHz ARM/1GHz DSP is 5 to 10W (depending on peripheral use and temperature)

4. C6-Integraprocessors include support for clock gatingfor each module on chip.

5. C6-Integraprocessors use three (3) power domains to support power gating. One (1) additional power domain is always on. The memory power domain supports light sleep, deep sleep, shut down modes.

6. C6-Integraprocessors support multiple supply voltages in the same ranges indicated in #2 (0.9V, 1V AVS (SmartReflex Technology), 1V constant, 1.5V, 1.8V, and 3.3V).

7. C6-Integraprocessors use Texas Instruments' Smart Reflex Technology and scaling the PLLs separately to support both voltage and frequency scaling.

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8. C6-Integraprocessors include the following hardware accelerators:

- HDVPSS (HD Video Processing SubSystem) w/ Media Controller
- 3D Graphics (SGX530)
- ELM (Error Locator Module) – accelerates NAND ECC.
- EDMA

9. C6-Integraprocessors do not support multithreading or hardware context switching.

10. Multiprocessing support consists of a C674x DSP coupled with an ARM Cortex-A8 that use an internal shared memory, HW mailbox and spinlocks. Software development is supported by the C6EZAccel & C6EZRun software development tools (EZ Tools).

11. Additional information for:

A. Making your code faster:

- The C6A816x C6-Integra is a multicore engine with dedicated support for heavy signal processing and control/connectivity functions. The main ARM core can run at top speeds of up to 1.5GHz. TI offers industry-standard APIs that can offload media processing tasks that tend to be the heaviest loads on the system.
- The C6A816x C6-Integra features the NEON vector floating-point engine and a dedicated graphics processor. The compiler tools allow easy speed-up of the code that can use the vector FP capabilities of Neon. The media portions of the application can use industry standard OpenMax and OpenGL APIs to speed up processing.

B. Using the hardware accelerators

- The C6A816x C6-Integra supports dedicated HW acceleration for graphics. 3D graphics is offloaded into dedicated 2D/3D graphics engines that provide OpenGL and OpenVG acceleration.

C. No additional information for sleep and idle modes

D. Optimize the locality of memory

- The C6A816x C6-Integra features advanced capabilities that organizes local memory to maximize the throughput of the memory sub-system.

- The C6A816x C6-Integra features advanced dedicated HW systems that can organize the normal raster memory into tiles that are extremely efficient for data management and transfer.
- The C6A816x C6-Integra features an advanced dynamic memory manager HW module that can organize, prioritize and re-order memory transactions in a manner that maximizes the utilization of the memory throughput.

E. Using buffers and pre-allocated resources

- The C6A816x C6-Integra offers dynamic resource management capabilities that allow flexible allocation of HW to applications. Memory allocations can be dynamic, driven by system use-cases, and/or centrally managed by the Host operating system.
- The HW resources for media processing and signal processing can also be centrally managed by the host operating system and allocated across the various applications dynamically.
- TI's software also features the Syslink driver which allows a flexible management of all the HW co-processors and the memory needed by them.

F. Optimize data movement

- The C6A816x C6-Integra offers a system enhanced DMA engine that can be used flexibly by the host or one of the several co-processors if desired. Other DMA engines in the system manage the transfer of data across PCIe and Ethernet.

G. Optimize interrupt handling

- TI's software architecture allows offloading of interrupt handling tasks to the co-processor engines. As an example, scaling and displaying multiple channels of HD media in the system would involve servicing many interrupts per second simply to keep the media engine going. Doing this on the host will kill its performance and leave no room for the host application or other tasks. Offloading this to a slave processor that uses a real-time operating system to service and handle the interrupts keeps the HW engines at maximum throughput.

H. Manage multi-threading

- The asymmetric multicore engine can offload media threads to other slave processors to free the host processor to focus on host tasks.